A NOVEL HIGH EFFICIENCY MULTIOCTAVE AMPLIFIER USING CASCADED REACTIVELY TERMINATED SINGLE-STAGE DISTRIBUTED AMPLIFIERS FOR EW SYSTEM APPLICATIONS

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ABSTRACT

This paper demonstrates the design of a high efficiency amplifier employing a novel concept of cascaded reactively terminated single-stage distributed amplifier (CRTSSDA). In addition, CRTSSDA produces an available power gain significantly higher than conventional distributed amplifiers using the same number of active devices. Three-CRTSSDAs were designed and fabricated for EW application. The novel amplifier achieved an associated gain above 26 dB with flatness of < ±0.5 dB, an average power added efficiency in access of 27% at an output power of 25 dBm over the 2-18 GHz with an efficiency peak of 30% at 12 GHz.

I. INTRODUCTION

Electronic warfare applications or phase array radar require wide and narrow band amplifiers where both high power and efficiency are desired simultaneously. Distributed amplifiers have been extensively investigated previously [1]. They have dominated broadband amplifier design for the last two decades and provide an excellent method for realising amplifiers for multioctave band applications. The best reported [2][3] power added efficiency performance achieved over 2-18 GHz bandwidth has been about 15% to 17%. It has been previously been shown that the concept of CRTSSDA configuration offers the realisation of high gain amplifiers, however over a limited bandwidth [4]. Moreover, simulation results presented in reference [5] show that with modifications to the CRTSSDA circuit, the CRTSSDA can provide an improved power added efficiency advantage over the conventional distributed amplifiers. This paper describes the design and measured performance of a three-CRTSSDA using DPHEMT devices for realising both high gain and high efficiency performance over a wide bandwidth (2-18 GHz).

II. CIRCUIT DESIGN METHOD

The schematic circuit diagram of the proposed cascaded reactively terminated single-stage amplifier (CRTSSDA), shown in Figure 1, is based on the principle of cascading T-section network of amplifiers in series. The signal power injected at the matched input generator port is coupled and amplified by the transconductance of the active device at each stage, and finally terminated by the matched output load port. At each stage, the signal power can be improved by terminating with a properly matched load resistor. The CRTSSDA configuration has the advantage over the conventional distributed amplifier in that it does not require any phase equalisation due to the fact that the total output current is not dependent on the phase coherence of the individual current generators. The only requirement is to equalise the characteristic impedance of the input gate and the output drain port of the active devices employed. The gate and drain inductance present in the circuit however limits the amplifier bandwidth performance. It is shown here that the bandwidth limitation can be compensated by the inclusion of the

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inductance, L_{var}, and resistance, R_{var}, as shown in Figure 1. The selection of the bias components L_{bias} and C_{bias} also play a critical role in optimising the bandwidth. These components should be chosen for minimum intrinsic parasitic components in order to avoid in-band resonance. Figure 2 shows the equivalent diagram of the *n*-cascaded reactively terminated single-stage distributed amplifiers. This circuit has internal stages of characteristic impedance Z_{int}, represented by the reactive elements $Z(\omega) = R_{var}(\omega) + j\omega L_{var}(\omega)$, and the input and output characteristic impedance Z_o. The output voltage at the *(n-1)* stage is given by [4]:

$$V_{o(n-1)} = \frac{1}{2} g_m^{(n-1)} Z_{int}^{(n-1)} E_s \qquad (1)$$

The output voltage at stage *n* is:

$$V_{on} = \frac{1}{2} g_m V_{o(n-1)} Z_o \qquad (2)$$

Therefore from equations (1) and (2) we have:

$$V_{on} = \frac{1}{4} g_m^{n} Z_{int}^{(n-1)} Z_o E_s \qquad (3)$$

The power delivered to a matched load is:

$$P_{out} = \frac{V_{on}^2}{Z_o} \qquad (4)$$

Power available from the generator is given by:

$$P_{in} = \frac{E_s^2}{4 Z_o} \qquad (5)$$

Power available from the generator is given by:

$$G_{cas} = \frac{Power\ available\ at\ the\ output}{Power\ available\ from\ the\ generato} \qquad (6)$$

The single-stages are cascaded in series so that the signal propagates forward from the input to the output ports. The gain for the ideal loss less *n*-CRTSSDA is therefore given by:

$$G_{cas} = \frac{1}{4} g_m^{2n} Z_{int}^{2(n-1)} Z_o^2 \qquad (7)$$

Equation (7) shows that substantially higher gain level can be realised from the CRTSSDA configuration. The output power and efficiency of the amplifier can be further improved by incorporating a large signal impedance matching network, represented by the impedance transformer (n:1) at the output of device T3, as illustrated in Figure 2. Low cut-off frequency (f_{min}) performance of the amplifier is determined by the components L_{bias} and C_{bias}, and can be determined from the following equations:

$$L_{bias} = \frac{25}{f_{min}(GHz)} (nH) \qquad (8)$$

and

$$C_{bias} = \frac{150}{f_{min}(GHz)} (pF) \qquad (9)$$

III. AMPLIFIER DESIGN

Devices LPD200, LP6836 and LP6872 manufactured by Filtronic Solid State, which have gate length of 0.25µm and gate widths of 200µm, 360µm and 720µm, respectively, were employed. Small- and large-signal models for these devices were developed using the CAD program LIBRA®. The design of the 3-CRTSSDA began with the calculation, using equation (7) of the number of devices required to achieve a gain level of 26 dB. Three-active devices were required to achieve the required gain. LIBRA® was used to carry out the small- and large-signal simulation and optimisation of the 3-CRTSSDA design. The optimised small-signal response of the amplifier is shown in Figure 3. The predicted gain level was 27 ± 1 dB and the input return loss was better than 2:1. Figure 4 shows the optimised large-signal simulation of the amplifier for output power. Figure 5 shows the predicted power added efficiency over 2-18 GHz.

IV. AMPLIFIER FABRICATION

The three-CRTSSDA was fabricated on 15 mil thick alumina substrate ($\varepsilon_r = 9.8$). The circuit layout is shown in Figure 6. Thin-film resistors were realised by etching into the nichrome layer. Chip components were soldered and all the electrical connections were carried out using 0.7 mil diameter gold wires. The inductors were fabricated using 1 mil diameter gold wire. The miniature gold coils had the appropriate number of turns to realise the inductance's required.

V. AMPLIFIER PERFORMANCE

The measured small-signal gain and input return loss of the three-CRTSSDA is shown in Figure 3. The measured gain was 26.5 ± 1.0 dB with a flatness of $< \pm 0.5$ dB, and the input return loss was better than 9.6 dB (i.e. VSWRs of better than 2:1). The measured output power, shown in Figure 4, was greater than 24.5 dBm. Figure 5 shows that the power added efficiency was greater than 27% across 2-18 GHz. A comparison of the measured results with the simulated responses shows excellent agreement.

VI. CONCLUSION

This paper demonstrates the design of a high efficiency power amplifier using the concept of cascaded reactively terminated single-stage distributed amplifier (CRTSSDA). The average measured PAE was 27% at an average output power of 25 dBm over 2-18 GHz. The CRTSSDA design implemented demonstrates the realisation of wide band power amplifiers having both high gain and high PAE.

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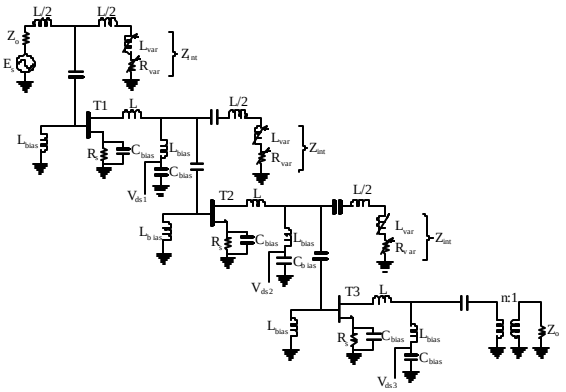

Figure 1 3-CRTSSDA Circuit Schematic

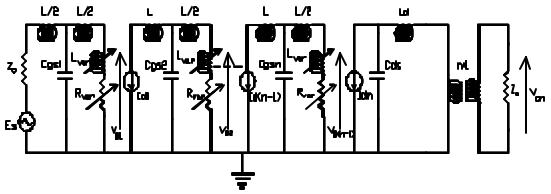

Figure 2 Equivalent Circuit Diagram of n-CRTSSDA

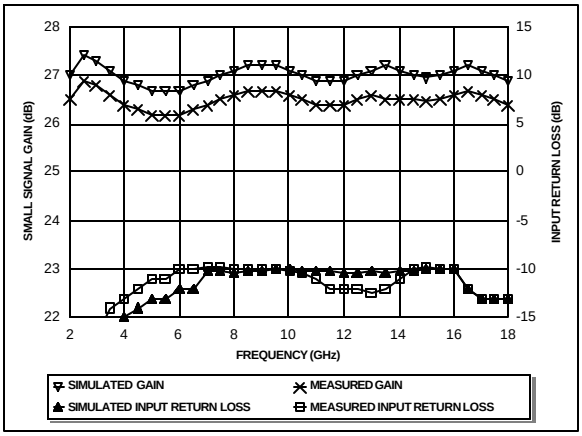

Figure 3 Simulated and Measured 3-CRTSSDA Small-Signal Response

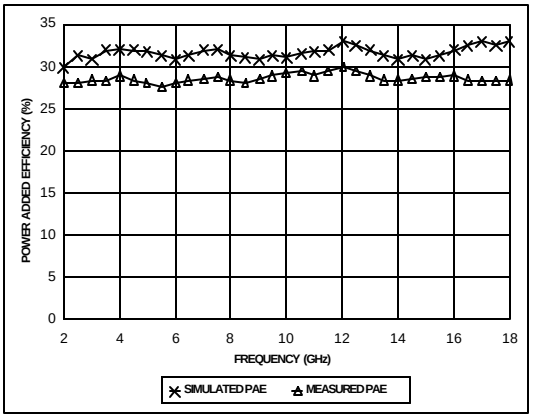

Figure 5 Simulated & Measured 3-CRTSSDA Power Added Efficiency

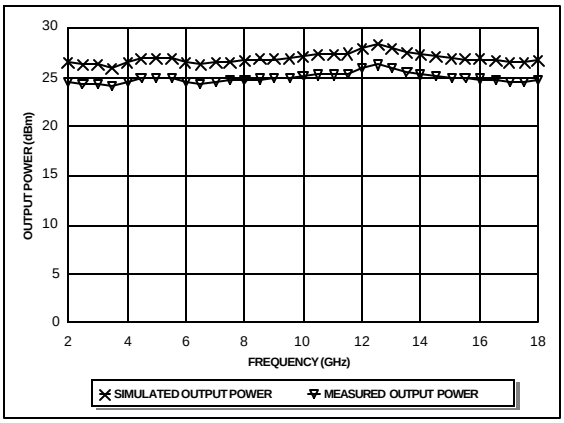

Figure 4 Simulated and Measured 3-CRTSSDA Output Power

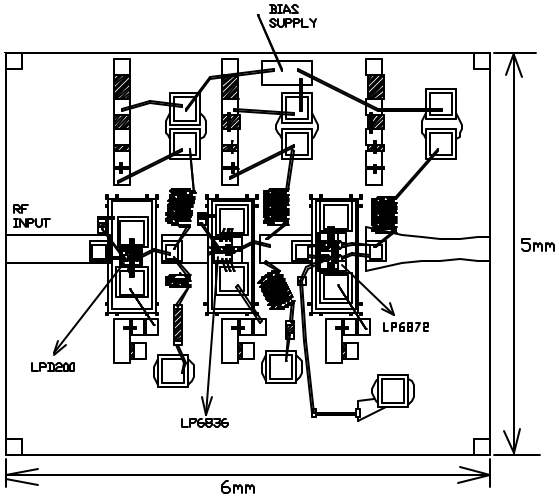

Figure 6 3-CRTSSDA Assembly